What is claimed is:

1. A memory cache bank prediction unit for use in a processor having a plurality of memory cache banks, comprising:

an input port configured to receive an instruction; and

an evaluation unit coupled to said input port and configured to predict which of the plurality of memory cache banks is associated with the instruction.

2. The memory cache bank prediction unit of claim 1, wherein said evaluation unit is configured to predict which of the plurality of memory cache banks is associated with the instruction based on information related to at least one of: (I) a bank history; (ii) a control flow; and (iii) a load target-address information.

3. The memory cache bank prediction unit of claim 1, wherein said evaluation unit is configured to perform a plurality of binary evaluations and predict which of the plurality of memory cache banks is associated with the instruction based on a majority vote of the plurality of binary evaluations.

4. The memory cache bank prediction unit of claim 1, wherein said evaluation unit is configured to perform a plurality of evaluations, each evaluation being associated with a confidence, and predict which of the plurality of memory cache banks is associated with the instruction based on the plurality of evaluation confidences.

5. The memory cache bank prediction unit of claim 4, wherein said evaluation unit is configured to predict which of the plurality of memory cache banks is associated with the instruction based on obtaining a sum of evaluation confidences above a threshold value.

6. A method of scheduling an instruction to a processor having a plurality of memory cache banks, comprising:

predicting which of the plurality of memory cache banks is associated with the instruction; and

scheduling the instruction for execution based on the predicted memory cache bank.

7. The method of claim 6, wherein said predicting is based on information related to at least one of: (I) a bank history; (ii) a control flow; and (iii) a load target-address information.

8. The method of claim 6, wherein said predicting comprises performing a plurality of binary evaluations and the prediction is based on a majority vote of the plurality of binary evaluations.

9. The method of claim 6, wherein said predicting comprises a plurality of evaluations, each evaluation being associated with a confidence, and the prediction is based on the plurality of evaluation confidences.

10. The method of claim 9, wherein said predicting is based on a sum of evaluation confidences above a threshold value.

11. An article of manufacture comprising a computer-readable medium having stored thereon instructions adapted to be executed by a processor having a plurality of memory cache banks, the instructions which, when executed, cause the processor to schedule an instruction, comprising:

predicting which of the plurality of memory cache banks is associated with the instruction; and

scheduling the instruction for execution based on the predicted memory cache bank.

12. A processor having a first memory cache bank and a second memory cache bank, comprising:

a memory cache bank prediction unit configured to predict which of the plurality of memory cache banks is associated with an instruction; and

a scheduler coupled to said memory cache bank prediction unit and configured to schedule the instruction for execution based on the predicted memory cache bank.

13. A processor having a first memory cache bank and a second memory cache bank, comprising:

a memory cache bank prediction unit;

a scheduler coupled to said memory cache bank prediction unit;

a first instruction pipeline between said scheduler and the first memory cache bank; and

a second instruction pipeline between said scheduler and the second memory cache bank;

wherein an instruction is placed in both said first instruction pipeline and said instruction pipeline.

14. The processor of claim 13, wherein instructions in the first pipeline are unable to access information in the second memory cache bank and instruction in the second pipeline are unable to access information the first memory cache bank.

15. The processor of claim 14, wherein an instruction in the first instruction pipeline is discarded if it needs to access information in the second memory cache bank.

16. The processor of claim 13, wherein said prediction unit predicts based on information related to at least one of: (I) a bank history; (ii) a control flow; and (iii) a load target-address information.

17. The processor of claim 13, wherein said prediction unit performs a plurality of binary evaluations and the prediction is based on a majority vote of the plurality of binary evaluations.

18. The processor of claim 13, wherein said prediction unit performs a plurality of evaluations, each evaluation being associated with a confidence, and the prediction is based on the plurality of evaluation confidences.

19. The processor of claim 18, wherein said prediction unit predicts based on a sum of evaluation confidences above a threshold value.

20. A method of executing an instruction in a processor having (I) a first instruction pipeline between a scheduler and a first memory cache bank and (ii) a second instruction pipeline between the scheduler and a second memory cache bank, comprising:

predicting which of the memory cache banks is associated with the instruction; and

processing the instruction in both the first instruction pipeline and the second instruction pipeline.

21. An article of manufacture comprising a computer-readable medium having stored thereon instructions adapted to be executed by a processor having (I) a first instruction pipeline between a scheduler and a first memory cache bank and (ii) a second instruction pipeline between the scheduler and a second memory cache bank, the instructions which, when executed, cause the processor to execute an instruction, comprising:

processing the instruction in both the first instruction pipeline and the second instruction pipeline.